TEST REPORT

Engineering Recommendation G83 Issue 2 (December 2012) Recommendations For The Connection Of Type Tested Small-Scale Embedded Generators (Up To 16A Per Phase) In Parallel With Low-Voltage Distribution Systems

Report reference No. ..... :	140327083GZU-002
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Date of issue ..... :	30 May 2014
Contents ..... :	24 Pages
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Testing location ..... :	Same as above
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Applicant's Name ..... :	Shenzhen SOFARSOLAR Co., Ltd.
Address ..... :	3A-1, Huake Building, East Technology Park, Qiaoxiang Road, Nanshan District, Shenzhen, China
Test specification	
Standard ..... :	G83 Issue 2 : 2012
Test procedure ..... :	Type test
Non-standard test method ..... :	N/A
Test Report Form No. ..... :	G83/2[a]
TTRF originator . ..... :	Intertek
Master TRF ..... :	dated 2013-07
Test item description ..... :	Grid-interactive PV inverter
Trademark ..... :	SOFAR SOLAR
Manufacturer ..... :	Same as applicant
Factory ..... :	Dongguan dingqiang Machinery & Electric Co., Ltd. No. 8, Fulong road, Qingxi town, Dongguan city, Guangdong, China
Model and/or type reference ..... :	Sofar 10000TL-Sx (x=0-6) （refer to General product information for details）
Rating(s) ..... :	Maximum d.c. input voltage: 1000 V Input voltage rang: 250-960 V Max. Input current: 2×15 A Max. PV Isc: 2×20 A Nominal Grid voltage: 3/N/PE230V/400V Max. Output current: 3×15 A

	Nominal Grid frequency: 50 Hz Max. Output power: 10000 W Ingress protection: IP65 Operating temperature range: -25～60℃
Summary of testing: The sample(s) tested complied with the type test requirement of G83 Issue 2: 2012	
Test case verdicts	
Test case does not apply to the test object .:	N/A
Test item does meet the requirement .....:	P(ass)
Test item does not meet the requirement ...:	F(ail)
Testing	
Date of receipt of test item .....:	27 Mar 2014
Date(s) of performance of test .....:	27 Mar 2014 – 09 May 2014

General remarks

The test results presented in this report relate only to the object tested.
This report shall not be reproduced, except in full, without the written approval of the Issuing testing laboratory.
"(See Enclosure #)" refers to additional information appended to the report.
"(See appended table)" refers to a table appended to the report.

Throughout this report a point is used as the decimal separator.

When determining the test conclusion, the Measurement Uncertainty of test has been considered.

General product information:

1. Product covered by this report is non-isolated grid-connected PV inverter for connection with low voltage grid in terms of G83-2.
2. The inverters intended to operate at ambient temperature -25℃ - +60℃ and 250-960 Vdc input, which will be specified in the user manual, The inverters will output full power when operated at 45℃. If operated at higher than 45℃ temperature, the output power derating.
3. if the DC input voltage is higher than 850 Vdc the output power will be derating; if the DC input voltage is lower than 350 Vdc, the output power will be derating.

"x" of model Sofar 10000TL-Sx denotes number from "0" to "6", and difference as following:

Model	DC Cable Gland	PV connector	DC inside connector	Fuse PCB+ String detection board	DC surge arrester	DC switch	AC switch	AC surge arrester
Sofar 10000TL-S0	√		√					
Sofar 10000TL-S1	√		√			√		
Sofar 10000TL-S2		√	√			√		
Sofar 10000TL-S3		√		√		√		
Sofar 10000TL-S4		√		√	√	√		
Sofar 10000TL-S5		√		√	√	√		√
Sofar 10000TL-S6		√		√	√	√	√	√
√ denote incorporating this component								

The product was tested on Software version: V1.00

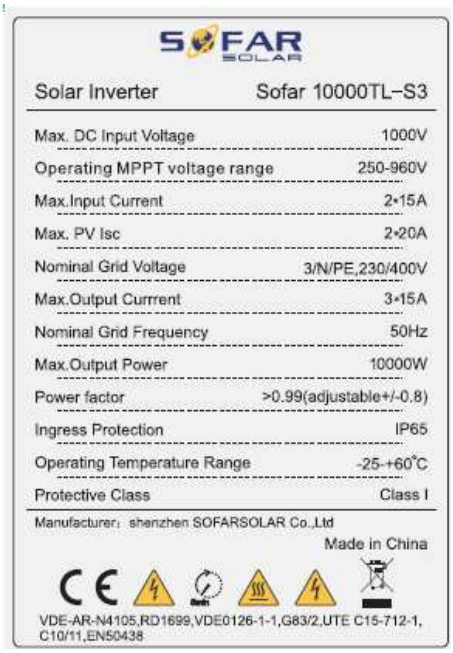
Other than special note, model Sofar 10000TL-S6 used for testing.

Software setting as following:

Different country can be set on switch SWT3 on communication board, digit "0" represents OFF, digit "1" represents ON

SWITCH 5	SWITCH 4	SWITCH 3	SWITCH 2	SWITCH 1	Country
1	0	0	0	0	UK-G83

Copy of marking plate:



Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation

Engineering recommendation G83/2			
Clause	Requirement – Test	Result – Remark	Verdict
5	Connection, Protection & Testing Requirements		P
5.1	Connection Procedure		N/A
5.2	Installation Wiring and Isolation		N/A
5.3	Interface Protection	Integrated into SSEG	P
5.3.1	Interface Protection Settings and Test Requirements	See table 5.3.1	P
	Interface Protection shall be installed which disconnects the SSEG system from the DNO's Distribution System when any parameter is outside of the settings shown in Table 1.		P
	The total disconnection time for voltage and frequency protection including the operating time of the disconnection device shall be the trip delay setting with a tolerance of, -0 s + 0.5s.		P
	All settings shall be applied as shown in the above table, so that they can be inspected if required by the DNO to confirm that the settings are correct.		P
	Only devices that have protection settings set and locked during manufacture can be considered as Type Tested		P
	The Manufacturer needs to establish a secure way of displaying the settings in one of the following ways.	The way (b) applied	P
	a) A display on a screen which can be read; b) A display on a PC which can communicate with the device and confirm that it is the correct device by means of a serial number permanently fixed to the device and visible on the PC screen at the same time as the settings; c) Display of all settings including nominal voltage and current outputs, alongside the serial number of the device, permanently fixed to the device.		P
	The Manufacturer must ensure that the Interface Protection is capable of measuring voltage to an accuracy of ± 1.5% of the nominal value (± 3.45V) and of measuring frequency to ± 0.2% of the nominal value (± 0.1Hz) across its operating range of voltage, frequency and temperature.	See table 5.3.1	P
	In response to a protection operation the SSEG system shall be automatically disconnected from the DNO's Distribution System, this disconnection must be achieved preferably by the separation of mechanical contacts or alternatively by the operation of a suitably rated solid state switching device.	Two series relays	P
5.3.2	Loss of Mains Protection	See table 5.3.2	P

Engineering recommendation G83/2			
Clause	Requirement – Test	Result – Remark	Verdict
5.3.3	Frequency Drift and Step Change Stability Test	See table 5.3.3	P
5.3.4	Automatic Reconnection	See table 5.3.4	P
	the voltage and frequency on the DNO's Distribution System have remained within the limits of Table 1 for a minimum of 20 seconds		P
5.4	Quality of Supply		P
	the SSEG shall comply with the requirements of the EMC Directive and in particular the product family emission standards listed in Table 2.		P
5.4.1	Testing for Harmonic emissions	See table 5.4.1	P
5.4.2	Testing for flicker	See table 5.4.2	P
5.5	DC Injection	See table 5.5 and 5.6	P
	The upper limit for DC injection is 0.25% of AC current rating per phase		P
	Where necessary the DC emission requirements can also be satisfied by installing an isolating transformer between the Inverter and the connection to the DNO's Distribution System.		N/A
5.6	Power Factor	See table 5.5 and 5.6	P
	A power factor within the range 0.95 lagging to 0.95 leading	A Fixed power factor at range 0.95 lagging to 0.95 leading	P
5.7	Short Circuit Current Contribution	See table 5.7.2	--
5.7.1	Directly Coupled Generation	PV inverter	N/A
5.7.2	Inverter Connected Generation		P
5.8	Voltage Unbalance		N/A
5.9	Certification Requirements		P
6	Operation and Safety	CE marking	P
6.1	Operational Requirements		N/A
6.2	Labelling		N/A
6.3	Maintenance & Routine Testing	This information including in the installation and user instructions	P
	Periodic testing of the SSEG is recommended at intervals prescribed by the Manufacturer. This information shall be included in the installation and User Instructions.		P
6.4	Earthing	It is a non-isolated PV inverter	N/A
7	Commissioning/Decommissioning and Acceptance Testing		N/A
Appendix 1	Connection Procedure Flow Chart		N/A
Appendix 2	Application for Connection		N/A

Engineering recommendation G83/2			
Clause	Requirement – Test	Result – Remark	Verdict
Appendix 3	SSEG Installation Commissioning Confirmation		N/A
Appendix 4	Type Verification Test Report		N/A
Appendix 5	SSEG Decommissioning Confirmation		N/A
Appendix 6	Relaxation of Commissioning Notification Timescales for SSEG: HSE Certificate of Exemption (August 2008)		N/A
Annex A1	Common Inverter Requirements.		P
A1.1	Certification & Type Testing SSEG Requirements		P
A1.2	CE Marking and Certification	A label with CE marking	P
A1.3	Type Verification Functional Testing of the Interface Protection		P
A1.3.1	Disconnection times		P
A1.3.2	Over / Under Voltage		P
A1.3.3	Over / Under Frequency		P
A1.3.4	Loss of Mains Protection		P
A1.3.5	Re-connection		P
A1.3.6	Frequency Drift and Step Change Stability test.		P
A1.4	POWER QUALITY		P
A1.4.1	Harmonics		P
A1.4.2	Power Factor		P
A1.4.3	Voltage Flicker		P
A1.4.4	DC Injection		P
A1.4.5	Overcurrent Protection		N/A
A1.4.6	Short Circuit Current Contribution		P
A1.4.7	Self-Monitoring – Solid State Disconnection		N/A
A1.4.8	Electromagnetic Compatibility (EMC)		P
Annex B1	Common Directly Coupled Connected SSEG Requirements		P
Annex C1	Separate Specific SSEG Technology Requirements		N/A
	C1.2 Photovoltaic		P

Appendix 1: Testing table

Table 5.3.1 Protection. Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3					P	
Function	Setting		Trip test			
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.5Hz	20s	47.49Hz	20.027s	47.7Hz 25s	No trip
			47.49Hz	20.100s		
			47.48Hz	20.038s		
			47.49Hz	20.036s		
			47.49Hz	20.102s		
U/F stage 2	47Hz	0.5s	46.98Hz	0.521s	47.2Hz 19.98s	No trip
			46.95Hz	0.516s		
			46.98Hz	0.524s		
			46.99Hz	0.533s		
			46.98Hz	0.534s		
					46.8Hz 0.48s	No trip
O/F stage 1	51.5Hz	90s	51.51Hz	90.200s	51.3Hz 95s	No trip
			51.51Hz	90.036s		
			51.51Hz	90.026s		
			51.51Hz	90.044s		
			51.51Hz	90.042s		
O/F stage 2	52Hz	0.5s	52.01Hz	0.510s	51.8Hz 89.98s	No trip
			52.01Hz	0.524s		
			50.01Hz	0.523s		
			50.01Hz	0.531s		
			50.01Hz	0.526s		

Appendix 1: Testing table

					52.2Hz 0.48s	No trip
Operation of the under/over frequency protection will be demonstrated for an increase or decrease of frequency within ± 0.5% of the trip settings, e.g. for an Over Frequency setting of 50.5 Hz the permissible operating range is 50.5 ± 0.2525 Hz. The test frequency should be applied in steps of ± 0.5% of setting for a duration that is longer than the trip time delay, for example 1 second in the case of a delay setting of 0.5 second.						

Table 5.3.1 (Continue) Protection. Voltage tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						P
Function	Setting		Trip test		No trip tests	
	Voltage	Time delay	Voltage	Time delay	Voltage /time	Confirm no trip
U/V stage 1	200.1V	2.5s	R,S,T: 199.5V R: 199.6V S: 199.5V T: 199.6V	R,S,T: 2.52s R: 2.54s S: 2.53s T: 2.53s	204.1V 3.5s	No trip
			R,S,T: 199.6V R: 199.6V S: 199.5V T: 199.6V	R,S,T: 2.54s R: 2.54s S: 2.52s T: 2.52s		
			R,S,T: 199.5V R: 199.6V S: 199.5V T: 199.6V	R,S,T: 2.52s R: 2.54s S: 2.53s T: 2.53s		
			R,S,T: 199.5V R: 199.6V S: 199.5V T: 199.6V	R,S,T: 2.52s R: 2.54s S: 2.53s T: 2.53s		
			R,S,T: 199.5V R: 199.6V S: 199.5V T: 199.6V	R,S,T: 2.52s R: 2.53s S: 2.54s T: 2.53s		
U/V stage 2	184V	0.5s	R,S,T: 183.8V R: 183.8V S: 183.8V T: 183.7V	R,S,T: 0.528s R: 0.528s S: 0.528s T: 0.509s	188V 3.5s	No trip
			R,S,T: 183.8V R: 183.8V S: 183.8V T: 183.8V	R,S,T: 0.528s R: 0.528s S: 0.527s T: 0.524s		
			R,S,T: 183.8V R: 183.8V S: 183.8V T: 183.7V	R,S,T: 0.528s R: 0.526s S: 0.527s T: 0.524s		
			R,S,T: 183.8V R: 183.8V	R,S,T: 0.528s R: 0.533s		

Appendix 1: Testing table

			S: 183.8V T: 183.7V	S: 0.527s T: 0.529s		
			R,S,T: 183.7V R: 183.7V S: 183.8V T: 183.8V	R,S,T: 0.531s R: 0.528s S: 0.527s T: 0.534s		
					180V 0.48s	No trip
O/V stage 1	262.2V	1.0s	R,S,T: 262.0V R: 262.0V S: 262.1V T: 262.1V	R,S,T: 1.019s R: 1.018s S: 1.020s T: 1.014s	258.2V 2.0s	No trip
			R,S,T: 262.1V R: 262.1V S: 262.0V T: 262.0V	R,S,T: 1.021s R: 1.024s S: 1.020s T: 1.025s		
			R,S,T: 262.1V R: 262.0V S: 262.1V T: 262.1V	R,S,T: 1.025s R: 1.024s S: 1.023s T: 1.025s		
			R,S,T: 262.1V R: 262.1V S: 262.1V T: 262.0V	R,S,T: 1.022s R: 1.021s S: 1.022s T: 1.025s		
			R,S,T: 262.1V R: 262.0V S: 262.1V T: 262.1V	R,S,T: 1.021s R: 1.026s S: 1.020s T: 1.022s		
O/V stage 2	273.7V	0.5s	R,S,T: 273.2V R: 273.3V S: 273.2V T: 273.3V	R,S,T: 0.520s R: 0.530s S: 0.524s T: 0.526s	269.7V 0.98s	No trip
			R,S,T: 273.2V R: 273.3V S: 273.3V T: 273.3V	R,S,T: 0.520s R: 0.530s S: 0.524s T: 0.526s		
			R,S,T: 273.2V R: 273.2V S: 273.3V T: 273.3V	R,S,T: 0.524s R: 0.524s S: 0.526s T: 0.521s		
			R,S,T: 273.2V R: 273.2V S: 273.3V T: 273.3V	R,S,T: 0.524s R: 0.528s S: 0.526s T: 0.525s		
			R,S,T: 273.3V R: 273.3V S: 273.3V T: 273.3V	R,S,T: 0.524s R: 0.528s S: 0.526s T: 0.522s		

Appendix 1: Testing table

					277.7V 0.48s	No trip
Note for Voltage tests the Voltage required to trip is the setting ±3.45V. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting ±4V and for the relevant times as shown in the table above to ensure that the protection will not trip in error.						

Table 5.3.2 LOSS OF MAINS TEST (According to BS EN 62116)									P
No.	P EUT	QL	P AC	Q AC	Time (ms)	P EUT(w)	Qf	V DC	Remarks
1.	100	100	0	0	211	10000	1.00	800	Test A at BL
2.	66	66	0	0	248	6600	1.00	600	Test B at BL
3.	33	33	0	0	466	3300	1.00	300	Test C at BL
4.	100	100	-5	-5	124	10000	1.00	800	Test A at IB
5.	100	100	-5	0	158	10000	1.05	800	Test A at IB
6.	100	100	-5	+5	140	10000	1.10	800	Test A at IB
7.	100	100	0	-5	120	10000	0.95	800	Test A at IB
8.	100	100	0	+5	117	10000	1.05	800	Test A at IB
9.	100	100	+5	-5	148	10000	0.90	800	Test A at IB
10.	100	100	+5	0	179	10000	0.95	800	Test A at IB
11.	100	100	+5	+5	121	10000	1.00	800	Test A at IB
12.	66	66	0	-5	220	6600	0.95	600	Test B at IB
13.	66	66	0	-4	238	6600	0.96	600	Test B at IB
14.	66	66	0	-3	179	6600	0.97	600	Test B at IB
15.	66	66	0	-2	153	6600	0.98	600	Test B at IB
16.	66	66	0	-1	102	6600	0.99	600	Test B at IB
17.	66	66	0	1	234	6600	1.01	600	Test B at IB
18.	66	66	0	2	238	6600	1.02	600	Test B at IB
19.	66	66	0	3	210	6600	1.03	600	Test B at IB
20.	66	66	0	4	246	6600	1.04	600	Test B at IB
21.	66	66	0	5	191	6600	1.05	600	Test C at IB
22.	33	33	0	-5	156	3300	0.95	300	Test C at IB

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23.	33	33	0	-4	186	3300	0.96	300	Test C at IB
24.	33	33	0	-3	210	3300	0.97	300	Test C at IB
25.	33	33	0	-2	197	3300	0.98	300	Test C at IB
26.	33	33	0	-1	199	3300	0.99	300	Test C at IB
27.	33	33	0	1	94	3300	1.01	300	Test C at IB
28.	33	33	0	2	132	3300	1.02	300	Test C at IB
29.	33	33	0	3	210	3300	1.03	300	Test C at IB
30.	33	33	0	4	244	3300	1.04	300	Test C at IB
31.	33	33	0	5	226	3300	1.05	300	Test C at IB

Note:
Inverter connected to a network combining a resonant circuit with a Q factor = 1 and a variable load; the value of the load is to match the inverter output to within +/-5%. A switch is placed between inverter/load and distribution system.

Table 5.3.3 Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6				P
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		No trip
Negative Vector Shift	50.5Hz	- 9 degrees		No trip
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	No trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	No trip

Table 5.3.4 Protection. Re-connection timer. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5					P
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.					
Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
20s	33.35s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.		Not reconnection	Not reconnection	Not reconnection	Not reconnection

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Table 5.4.1 Harmonics						P
SSEG rating per phase R (rpp)			3.333kW		NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV)	Normalised Value (NV)	Measured Value (MV)	Normalised Value (NV)	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.0610	0.0674	0.0678	0.0749	1.080	
3	0.0146	0.0161	0.0221	0.0243	2.300	
4	0.0500	0.0552	0.0398	0.0440	0.430	
5	0.1804	0.1992	0.2587	0.2856	1.140	
6	0.0020	0.0022	0.0018	0.0020	0.300	
7	0.0581	0.0641	0.1633	0.1802	0.770	
8	0.0161	0.0178	0.0059	0.0065	0.230	
9	0.0077	0.0086	0.0112	0.0124	0.400	
10	0.0127	0.0140	0.0126	0.0139	0.184	
11	0.0291	0.0321	0.0362	0.0399	0.330	
12	0.0015	0.0017	0.0016	0.0018	0.153	
13	0.0320	0.0354	0.0396	0.0438	0.210	
14	0.0078	0.0086	0.0111	0.0122	0.131	
15	0.0030	0.0034	0.0028	0.0031	0.150	
16	0.0061	0.0067	0.0081	0.0090	0.115	

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17	0.0248	0.0274	0.0369	0.0408	0.132	
18	0.0013	0.0014	0.0011	0.0012	0.102	
19	0.0239	0.0264	0.0282	0.0311	0.118	
20	0.0029	0.0032	0.0080	0.0088	0.092	
21	0.0020	0.0022	0.0025	0.0028	0.107	0.160
22	0.0013	0.0014	0.0067	0.0074	0.084	
23	0.0182	0.0201	0.0220	0.0243	0.098	0.147
24	0.0009	0.0010	0.0011	0.0012	0.077	
25	0.0140	0.0155	0.0222	0.0245	0.090	0.135
26	0.0030	0.0033	0.0054	0.0060	0.071	
27	0.0014	0.0015	0.0016	0.0017	0.083	0.124
28	0.0043	0.0047	0.0045	0.0050	0.066	
29	0.0070	0.0077	0.0183	0.0202	0.078	0.117
30	0.0008	0.0009	0.0007	0.0008	0.061	
31	0.0049	0.0054	0.0158	0.0175	0.073	0.109
32	0.0037	0.0041	0.0024	0.0027	0.058	
33	0.0012	0.0014	0.0018	0.0020	0.068	0.102
34	0.0045	0.0049	0.0021	0.0023	0.054	
35	0.0019	0.0021	0.0131	0.0144	0.064	0.096

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36	0.0029	0.0032	0.0133	0.0147	0.051	
37	0.0024	0.0027	0.0009	0.0009	0.061	0.091
38	0.0017	0.0018	0.0013	0.0014	0.048	
39	0.0022	0.0024	0.0009	0.0010	0.058	0.087
40	0.0029	0.0032	0.0133	0.0147	0.046	
SSEG rating per phase S (rpp)			3.333kW		NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV)	Normalised Value (NV)	Measured Value (MV)	Normalised Value (NV)	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.0641	0.0708	0.0718	0.0792	1.080	
3	0.0177	0.0195	0.0161	0.0178	2.300	
4	0.0509	0.0562	0.0420	0.0463	0.430	
5	0.1960	0.2164	0.2967	0.3275	1.140	
6	0.0018	0.0020	0.0042	0.0047	0.300	
7	0.0561	0.0619	0.1562	0.1724	0.770	
8	0.0182	0.0201	0.0096	0.0106	0.230	
9	0.0213	0.0235	0.0314	0.0347	0.400	
10	0.0119	0.0132	0.0130	0.0144	0.184	
11	0.0277	0.0306	0.0428	0.0472	0.330	
12	0.0014	0.0016	0.0019	0.0021	0.153	
13	0.0335	0.0370	0.0371	0.0409	0.210	

Appendix 1: Testing table

14	0.0084	0.0092	0.0116	0.0128	0.131	
15	0.0119	0.0131	0.0081	0.0089	0.150	
16	0.0061	0.0067	0.0082	0.0090	0.115	
17	0.0256	0.0282	0.0382	0.0421	0.132	
18	0.0009	0.0010	0.0010	0.0011	0.102	
19	0.0248	0.0273	0.0275	0.0303	0.118	
20	0.0030	0.0033	0.0086	0.0095	0.092	
21	0.0030	0.0033	0.0036	0.0040	0.107	0.160
22	0.0008	0.0009	0.0056	0.0062	0.084	
23	0.0192	0.0212	0.0220	0.0243	0.098	0.147
24	0.0008	0.0009	0.0009	0.0010	0.077	
25	0.0144	0.0159	0.0211	0.0233	0.090	0.135
26	0.0030	0.0033	0.0058	0.0064	0.071	
27	0.0027	0.0030	0.0022	0.0024	0.083	0.124
28	0.0038	0.0042	0.0039	0.0043	0.066	
29	0.0072	0.0079	0.0180	0.0199	0.078	0.117
30	0.0006	0.0007	0.0008	0.0009	0.061	
31	0.0043	0.0048	0.0157	0.0174	0.073	0.109
32	0.0046	0.0051	0.0033	0.0037	0.058	

Appendix 1: Testing table

33	0.0030	0.0034	0.0019	0.0021	0.068	0.102
34	0.0043	0.0048	0.0020	0.0022	0.054	
35	0.0022	0.0024	0.0128	0.0142	0.064	0.096
36	0.0007	0.0008	0.0006	0.0006	0.051	
37	0.0026	0.0029	0.0139	0.0154	0.061	0.091
38	0.0031	0.0035	0.0012	0.0013	0.048	
39	0.0015	0.0017	0.0023	0.0025	0.058	0.087
40	0.0022	0.0024	0.0008	0.0008	0.046	
SSEG rating per phase T (rpp)			3.333kW		NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV)	Normalised Value (NV)	Measured Value (MV)	Normalised Value (NV)	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.0560	0.0618	0.0659	0.0728	1.080	
3	0.0193	0.0213	0.0362	0.0400	2.300	
4	0.0500	0.0552	0.0373	0.0412	0.430	
5	0.1832	0.2023	0.2927	0.3232	1.140	
6	0.0021	0.0023	0.0041	0.0045	0.300	
7	0.0634	0.0700	0.1668	0.1842	0.770	
8	0.0176	0.0195	0.0093	0.0103	0.230	
9	0.0178	0.0196	0.0235	0.0260	0.400	
10	0.0109	0.0120	0.0126	0.0139	0.184	

Appendix 1: Testing table

11	0.0217	0.0240	0.0439	0.0484	0.330	
12	0.0013	0.0014	0.0018	0.0020	0.153	
13	0.0289	0.0319	0.0371	0.0410	0.210	
14	0.0083	0.0092	0.0112	0.0123	0.131	
15	0.0127	0.0140	0.0085	0.0094	0.150	
16	0.0049	0.0054	0.0077	0.0085	0.115	
17	0.0241	0.0266	0.0361	0.0399	0.132	
18	0.0009	0.0010	0.0010	0.0011	0.102	
19	0.0240	0.0265	0.0247	0.0273	0.118	
20	0.0038	0.0042	0.0084	0.0093	0.092	
21	0.0024	0.0026	0.0030	0.0033	0.107	0.160
22	0.0011	0.0012	0.0058	0.0064	0.084	
23	0.0184	0.0203	0.0228	0.0252	0.098	0.147
24	0.0010	0.0011	0.0013	0.0015	0.077	
25	0.0140	0.0155	0.0198	0.0218	0.090	0.135
26	0.0033	0.0036	0.0063	0.0070	0.071	
27	0.0016	0.0018	0.0016	0.0017	0.083	0.124
28	0.0038	0.0042	0.0036	0.0040	0.066	
29	0.0081	0.0090	0.0187	0.0207	0.078	0.117

Appendix 1: Testing table

30	0.0009	0.0009	0.0009	0.0010	0.061	
31	0.0050	0.0055	0.0139	0.0154	0.073	0.109
32	0.0048	0.0053	0.0032	0.0035	0.058	
33	0.0024	0.0027	0.0018	0.0020	0.068	0.102
34	0.0042	0.0046	0.0014	0.0016	0.054	
35	0.0015	0.0016	0.0129	0.0142	0.064	0.096
36	0.0007	0.0008	0.0006	0.0007	0.051	
37	0.0020	0.0023	0.0124	0.0137	0.061	0.091
38	0.0033	0.0036	0.0009	0.0010	0.048	
39	0.0015	0.0017	0.0017	0.0019	0.058	0.087
40	0.0024	0.0026	0.0009	0.0010	0.046	

Note: the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

Power Quality. Voltage fluctuations and Flicker. The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3

	Starting			Stopping			Running	
	d_{max}	d_c	$d_{(t)}$	d_{max}	d_c	$d_{(t)}$	P_{st}	P_{lt} 2 hours
Measured Values(%)	0.96	1.28	0	0.96	1.28	0	0.083	0.192
Normalised to standard impedance and 3.68kW for multiple units(%)	0.96	1.28	0	0.96	1.28	0	0.083	0.192
Limits set under BS EN 61000-3-2	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	1.0	0.65

Appendix 1: Testing table

Table 5.5 and 5.6						P
G83/2 Limit	**DC injection**			**Power factor**		
	0.25%, tested at three power levels			0.95 lag– 0.95 lead at three voltage levels, Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.		
Test level	10%	55%	100%	216.2V	230V	253V
Test value	R: 0.012A S: 0.0091 T:0.0048	R:0.0148 S:0.0045 T:0.0066	R:0.0128 S:0.0043 T:0.0050	R:0.9996 S:0.9997 T:0.9997	R:0.9996 S:0.9997 T:0.9997	R:0.9995 S:0.9996 T:0.9996

Appendix 1: Testing table

Table 5.7 Fault level contribution. The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6		
For an Inverter SSEG.		
Time after fault	Volts	Amps
20ms	31.9V	R: 23.0Apeak S: 19.0Apeak T: 22.5Apeak
100ms	30.0V	R: 23.5Apeak S: 19.0Apeak T: 23.5Apeak
250ms	23.0V	R: 23.5Apeak S: 22.5Apeak T: 23.5Apeak
500ms	23.0V	0
Time to trip	260ms	

SELF MONITORING – SOLID STATE SWITCHING	
Test	**N/A**
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volt within 0.5 sec.	**No** **(mechanical relays used)**

Appendix 2: Photos

Overview

Bottom view

Appendix 2: Photos

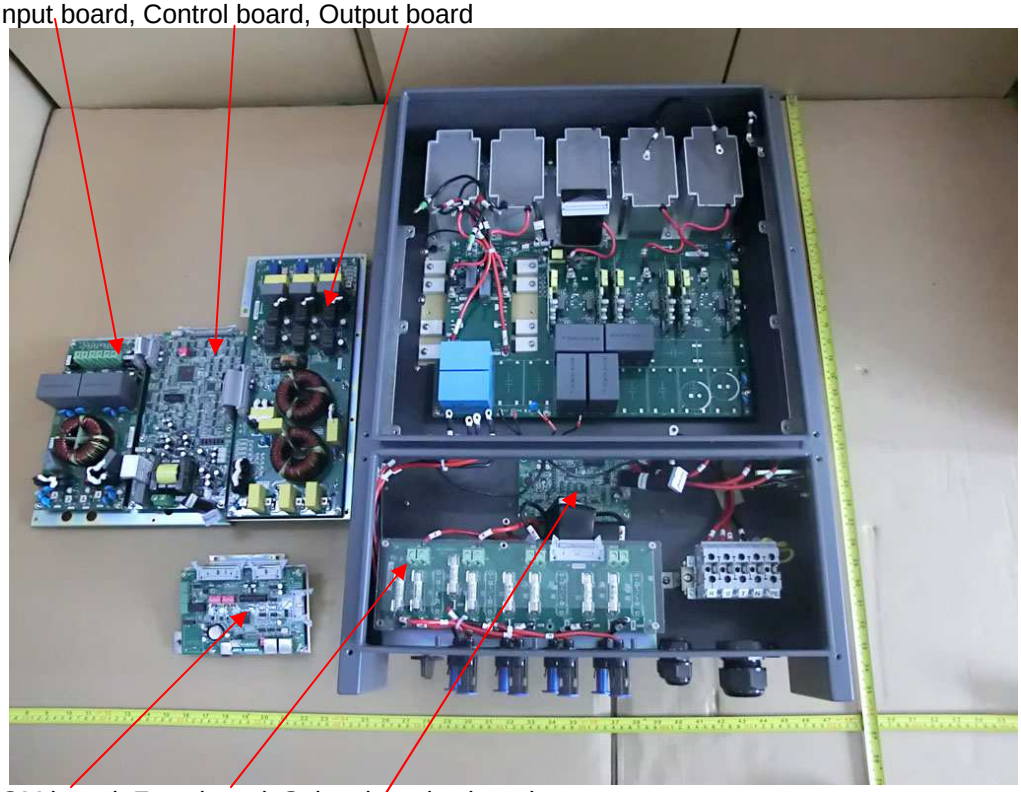
Terminal view

Internal view of the unit

Appendix 2: Photos

Internal view of the unit

Input board, Control board, Output board



COM board, Fuse board, String detection board

Internal view of the unit